

IN THE CLAIMS:

1 1. (CURRENTLY AMENDED) Apparatus for enhancing debug capability in a multiprocessor cir-
2 cuit, comprising:

3 a plurality of processors arranged so that data advances from processor to processor during
4 normal operation, each processor being a part of a processor complex that includes a first context
5 memory for data to be processed, and a second context memory for data that has been processed;

6 an advancement circuit, the advancement circuit configured to advance ~~enabling advance-~~
7 ~~ment of~~ data among the processors in the event of failure of a processor; and

8 a data bypass circuit configured to pass the data through the processor complex with past a
9 the failed one of the processors, by moving the data from the first context memory to the second
10 context memory of that processor complex absent processing.

1 2. (PREVIOUSLY PRESENTED) The apparatus as in claim 1, wherein said data bypass circuit
2 further comprises:

3 a bypass register.

1 3. (PREVIOUSLY PRESENTED) The apparatus as in claim 1, further comprising:

2 said plurality of processors arranged to process data as a pipeline.

1 4. (PREVIOUSLY PRESENTED) The apparatus as in claim 1, further comprising:

2 said plurality of processors arranged to process data as a pipeline; and

3 a bypass register, said bypass register having a bit location for each processor of the pipe-
4 line, each bit location capable of storing an override signal.

1 5. (CURRENTLY AMENDED) The apparatus as in claim 1, further comprising:

2 a memory, said memory storing computer code, said computer code having a code entry
3 point selected by said data bypass circuit to enable a downstream processor to do the work of a the
4 failed processor.

1 6. (CURRENTLY AMENDED) A method for enhancing debug capability in a multiprocessor
2 circuit, comprising:

3 advancing data among a plurality of processors, ~~the plurality of processors arranged so that~~
4 ~~data advances from processor to processor during normal operation~~ in response to completion sig-
5 nals from each of the processors;

6 advancing data among the processors ~~by an advancement circuit,~~ in the event of failure of a
7 processor in response to an override signal; and

8 passing the data through a processor complex including the past a failed one of the proces-
9 sors by a data bypass circuit moving data from a first context memory to a second context memory
10 of the processor complex absent processing.

1 7. (PREVIOUSLY PRESENTED) The method apparatus as in claim 6, further comprising:

2 indicating that a processor is to be bypassed by a bypass register.

1 8. (PREVIOUSLY PRESENTED) The method as in claim 6, further comprising:

2 arranging said plurality of processors to process data as a pipeline.

1 9. (CURRENTLY AMENDED) The method as in claim 6, further comprising:

2 arranging said plurality of processors to process data as a pipeline; and

3 storing an the override signal in a bit location of a bypass register.

1 10. (CURRENTLY AMENDED) The method as in claim 6, further comprising:

2 storing computer code in a memory, said computer code having a code entry point selected
3 by said data bypass circuit to enable a downstream processor to do the work of a the failed proces-
4 sor.

1 11. (CURRENTLY AMENDED) Apparatus for enhancing debug capability in a multiprocessor
2 circuit, comprising:

3 means for advancing data among a plurality of processors, ~~the plurality of processors ar-~~
4 ~~ranged so that data advances from processor to processor during normal operation in response to~~
5 completion signals from each of the processors;

6 means for advancing data among the processors ~~by an advancement circuit,~~ in the event of
7 failure of a processor in response to an override signal; and

8 means for passing the data through a processor complex including the past a failed one of
9 the processors by moving data from a first context memory to a second context memory of the
10 processor complex absent processing a data bypass circuit.

1 12. (CURRENTLY AMENDED) The apparatus as in claim 11, further comprising:

2 means for indicating that a processor is to be bypassed ~~by a bypass register.~~

1 13. (PREVIOUSLY PRESENTED) The apparatus as in claim 11, further comprising:

2 means for arranging said plurality of processors to process data as a pipeline.

1 14. (CURRENTLY AMENDED) The apparatus as in claim 11, further comprising:

2 means for arranging said plurality of processors to process data as a pipeline; and

3 means for storing an override signal in a bit location of a bypass register.

1 15. (CURRENTLY AMENDED) The apparatus as in claim 11, further comprising:

2 means for storing computer code ~~in a memory~~, said computer code having a code entry
3 point selected ~~by said data bypass circuit~~ to enable a downstream processor to do the work of a
4 failed processor.

1 16-17. (CANCELLED)

1 18. (NEW) Logic encoded on one or more tangible media for execution, and when executed oper-
2 able to:

1 advance data among a plurality of processors during normal operation in response to com-
2 pletion signals from each of the processors;

3 advance data among the processors in the event of failure of a processor in response to an
4 override signal; and

5 pass data through a processor complex including the failed one of the processors by moving
6 data from a first context memory to a second context memory of the processor complex absent
7 processing.